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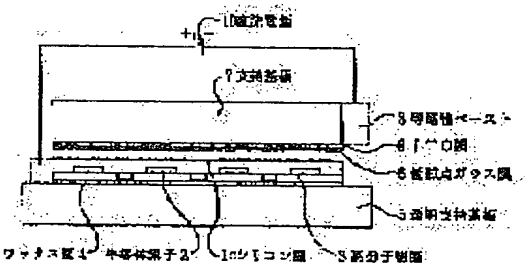
(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To provide a manufacturing method of a semiconductor device wherein a thinned substrate can be adhered to an insulating supporting substrate firmly without generating bubbles, etc., in an insulating supporting substrate regarding a manufacturing method of a semiconductor device wherein the thinned substrate is transcribed to another supporting substrate by forming a semiconductor device.
CONSTITUTION: After a semiconductor element 2 is formed in a surface of a silicon layer 1c of an SOI substrate, high polymer resin 3 is buried and flattened in a formation region of the semiconductor element 2 and the high polymer resin 3 and a transparent supporting substrate 5 are adhered. In a manufacturing process of a rear injection type infrared ray detection element wherein the insulator side of the SOT substrate at an opposite side of the formation region of the semiconductor element 2 is polished and the silicon layer 1c is thinned, the thinned silicon layer 1c is adhered to a supporting substrate 7 which has insulation property and transmits infrared ray at a normal temperature while applying a dc voltage through a low melting point glass film 6. The transparent supporting substrate 5 is peeled off from the high polymer resin 3 and the high polymer resin 3 is removed.



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* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] A silicon substrate or SOI substrate which prepared the silicon layer (1c) on the insulator (1a) (1) It is a semiconductor device (2) to the front face of said silicon layer (1c). After forming, Resin (3) is laid under this semiconductor device (2) formation field, and it is this semiconductor device (2). Flattening of the formation field is carried out. Said resin (3) and the transparence support substrate (5) which laid underground and carried out flattening of this semiconductor device (2) formation field It pastes up. Said semiconductor device (2) Said silicon substrate or said SOI substrate (1) of a formation field and the side which counters In the production process of the infrared detecting element of the rear-face incoming radiational type which grinds said insulator (1a) side and carries out lamination of the silicon layer (1c) Support substrate which has insulation for said silicon substrate which carried out lamination, or said silicon layer (1c), and penetrates infrared radiation (7) Low-melting-glass film (6) It minds. the process joined in ordinary temperature while impressing direct current voltage, and said semiconductor device (2) Said resin (3) laid underground from -- said transparence support substrate (5) Said resin (3) exfoliated and laid underground The manufacture approach of the semiconductor device characterized by including the process to remove.

[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]
[Industrial Application] This invention relates to a semi-conductor image sensor, the micro machine which formed minute machine parts, such as a gearing, by polish recon etc., especially relates to the manufacture approach of the semiconductor device which imprints the substrate which formed and carried out lamination of the semiconductor device to other support substrates.
[0002]
[Description of the Prior Art] In forming the semiconductor device of a CMOS mold in semi-conductor substrates, such as silicon, and manufacturing an infrared detecting element conventionally If incidence of the infrared radiation is carried out from the field side which silicon oxide, the electrode, the wiring layer, etc. are formed in this silicon substrate surface, and formed the semiconductor device of this silicon substrate Since infrared radiation is covered with an above-mentioned wiring layer and an above-mentioned electrode and incidence is not carried out to a semiconductor device formation field, in order to manufacture the infrared imaging detector of high sensitivity, the infrared detecting element of the rear-face incoming radiational type which carries out incidence of the infrared radiation from the rear-face side which does not form the semiconductor device of a silicon substrate is manufactured.
[0003] However, since the infrared radiation which carried out incidence from the rear-face side tends to be absorbed by the silicon substrate when the board thickness of a silicon substrate is thick, the board thickness of a silicon substrate is 10 micrometers. Although it must be made thin below, it is 10 micrometers about a silicon substrate in this way. If it is made the following sheet metal, it becomes easy to be divided and the problem that handling is difficult has arisen.
[0004] For this reason, conventionally, the approach which the board thickness which formed the semiconductor device 32 as shown in drawing 5 uses an epoxy resin 36 for the insulating support substrate 37 which consists the thin semi-conductor substrate 31 of sapphire which penetrates infrared radiation, and pastes up on it is adopted.
[0005]
[Problem(s) to be Solved by the Invention] Although the semi-conductor substrate is pasted up on the insulating support substrate which consists of sapphire which penetrates infrared radiation in the manufacture approach of the conventional semiconductor device explained above using adhesives as mentioned above It is very difficult technically to extend adhesives thinly to homogeneity and to paste up. Moreover, if the infrared imaging detector which air bubbles were easy to be formed in the interior of adhesives, and pasted the support substrate and manufactured the semi-conductor substrate in this way is put to the indoor temperature when not making it operate from the temperature of the liquid nitrogen of operating temperature The air in air bubbles expanded according to the temperature gradient, and there was a trouble that a crack occurred in adhesives.
[0006] This invention aims at offer of the manufacture approach of the semiconductor device which becomes possible [pasting up firmly] without generating air bubbles etc., in case the semi-conductor substrate which formed and carried out lamination of the semiconductor device from the above situations is pasted up on an insulating support substrate.
[0007]
[Means for Solving the Problem] After the manufacture approach of the semiconductor device of this invention forms a semiconductor device in the front face of this silicon layer of a silicon substrate or the SOI substrate which prepared the silicon layer on the insulator, Lay resin under this semiconductor device formation field, and flattening of this semiconductor device formation field is carried out. This resin and the transparence support substrate which laid underground and carried out flattening of this semiconductor device formation field are pasted up. In the production process of the infrared detecting element of the rear-face incoming radiational type which grinds said insulator side of this semiconductor device formation field, this silicon substrate of the side which counters, or this SOI substrate, and carries out lamination of the silicon layer The low-melting-glass film is support minded [which has insulation for said silicon substrate which carried out lamination, or said silicon layer, and penetrates infrared radiation]. Impressing direct current voltage, it constitutes so that the process which removes this resin

that exfoliated and laid this transparence support substrate underground from the process joined in ordinary temperature and this resin that laid this semiconductor device underground may be included.
[0008]
[Function] Namely, the semi-conductor layer which carried out lamination in this invention after forming a semiconductor device in one field of a semi-conductor layer, It becomes possible to paste up firmly, since the support substrate which has the same coefficient of thermal expansion as this semi-conductor layer, penetrates infrared radiation and has insulation is pasted up by ordinary temperature anode plate junction. When putting a semiconductor device to the room temperature of non-operating temperature from 77 degrees K of the liquid nitrogen temperature of operating temperature, it becomes possible to prevent that this semi-conductor layer exfoliates from a support substrate.
[0009] This ordinary temperature anode plate junction is "LoW-temperature Silicon-to-silicon Anodic Bonding with Intermediate LowMelting Point Glass, by MASAYOSHI ESASHI, AKIRA NAKANO, SHUICHI SHOJI andHIROYUKI HEBIGUCHI" of reference (Sensors and Actuators, A-21-A23 (1990) 931-934). It is set and indicated.
[0010] According to this reference, this approach puts the glass layer 16 on the silicon wafer 11 by the spatter, as while shows drawing 4 . If an electrical potential difference is impressed so that negative direct current voltage may be impressed to the silicon wafer 11 which was made to counter with the silicon wafer 21 on which another side should be pasted up, has arranged, and carried out the spatter of the glass layer 16 by DC power supply 20 Negative ion gathers in a part of glass layer 16 in which the spatter is carried out by the electric field of the impressed direct current voltage, and it is polarization field 16a. It is formed. It is the approach which it is drawn to the silicon wafer 21 of another side where the forward electrical potential difference is impressed by the negative ion in this polarization field, and silicon wafers paste up on it.
[0011] this invention -- setting -- this principle -- using -- drawing 1 (a) the support substrate 7 side becomes [an electrical potential difference] a conductor so that it may be shown and may be impressed certainly -- as -- the film of an indium, tin, and an oxide transparent on the front face of the support substrate 7 at conductivity (ITO) -- covering -- the front face of this ITO film 9 -- low melting glass (PbO-ZnO-B 2O3) from -- the becoming low-melting-glass film 6 is put.
[0012] And if the conductive paste 8 is applied to each side face of the support substrate 7 and silicon layer 1c, an electrical potential difference is impressed so that negative direct current voltage may be impressed to the support substrate 7 side which put the low-melting-glass film 6, and the low-melting-glass film 6 and silicon layer 1c are stuck by pressure, it is possible to paste up the support substrate 7 and silicon layer 1c.
[0013] Moreover, drawing 1 (b) When the low-melting-glass film 6 is formed in the front face of silicon layer 1c so that it may be shown, it is drawing 1 (a) about direct current voltage. A case can paste up the support substrate 7 and silicon layer 1c, if an electrical potential difference is impressed and the low-melting-glass film 6 and the ITO film 9 are stuck by pressure so that negative direct current voltage may be impressed to silicon layer 1c on the contrary.
[0014] Low melting glass used for this adhesion (PbO-ZnO-B 2O3) Membranous thickness is 1 micrometer which cannot be realized when pasting up in a resin layer. Since air bubbles do not remain like [it is possible to paste up in the layer of the following thickness, and / at the time of pasting up by resin], it does not exfoliate, even if it puts a semiconductor device to the non-operating temperature of a room temperature from 77 degrees K of the liquid nitrogen temperature of operating temperature.
[0015]
[Example] One example using the SOI substrate which formed the silicon layer on the silicon plate of this invention by drawing 1 - drawing 3 below is explained to a detail.
[0016] drawing in which drawing 1 shows the example of ordinary temperature anode plate junction of this invention, and sectional side elevation (1) showing the manufacture approach of the semiconductor device of one example according [drawing 2] to this invention in order of a process Sectional side elevation (2) showing the manufacture approach of the semiconductor

device of one example according [drawing 3] to this invention in order of a process it is .
[0017] It is drawing 2 (a) first. It is board thickness so that it may be shown. 400 micrometers It is 1 micrometer of thickness on silicon plate 1a. Silicon oxide 1b and 5-15 micrometers of thickness The SOI substrate 1 in which silicon layer 1c was formed, After forming a semiconductor device 2 in the silicon layer 1c side by the CMOS process, the macromolecule resin 3 which consists of polyimide resin (the Hitachi Chemical Co., Ltd. make, trade name-IQ) all over the formation field of this formed semiconductor device 2 is applied, and the formation field side of this semiconductor device 2 is made flat.
[0018] Next, it is drawing 2 (b). It pastes up using the wax which heated and fused the flat front face of the macromolecule resin 3 which has covered the formation field of this semiconductor device 2, and the transparence support substrate 5 which consists of a quartz so that it may be shown. The transparence support substrate 5 is used for finding and removing the air bubbles of the wax film 4, and ensuring adhesion here.
[0019] Subsequently, drawing 2 (c) It is abbreviation about silicon plate 1a of the SOI substrate 1 of the opposite side of the side which formed the semiconductor device 2 so that it might be shown. 360 micrometers Polish is stopped, just before grinding and reaching silicon oxide 1b. In etching using the etching reagent which consists of caustic potash until it reaches an interface with silicon oxide 1b of the SOI substrate 1 or dry etching -- residual silicon plate 1a -- removing -- ammonium fluoride (NH4F) Fluoric acid (HF) from -- silicon oxide 1b is removed using the becoming buffered fluoric acid.
[0020] Subsequently, drawing 3 (a) In order to give conductivity to the support substrate 7 with which silicon layer 1c in which this semiconductor device 2 was formed, and coefficient of thermal expansion agreed and which consists of sapphire so that it may be shown An indium, tin, and an oxide (it is hereafter called ITO for short.) from -- becoming thickness 0.3 micrometers The ITO layer 9 is formed by the spatter. It is thickness to the front face of this ITO layer 9. 0.5 micrometers Low melting glass (PbO-ZnO-B 2O3) Drawing 1 after forming the film 6 by the spatter (a) The side face of silicon layer 1c and the side face of the support substrate 7 are made to put the conductive paste 8, and it forms in them so that it may be shown.
[0021] The aforementioned low melting glass (PbO-ZnO-B 2O3) An electrical potential difference is impressed so that negative direct current voltage may be impressed to the support substrate 7 which put the film 6. If the direct current voltage of several 10 V is impressed by DC power supply 10 where an electrical potential difference is impressed so that forward direct current voltage may be impressed to the silicon layer 1c side, it will become possible to paste up firmly the ITO film 9 of the front face of the support substrate 7, and silicon layer 1c through the low-melting-glass film 6. Under the present circumstances, if a spindle is carried on a substrate and it pressurizes, it will become possible to make applied voltage low.
[0022] Then, it is immersed into the boiled pure water, the wax film 4 is softened, and it is drawing 3 (b). The transparence support substrate 5 is exfoliated from silicon layer 1c which carried out lamination so that it may be shown, and it is drawing 3 (c). The wax film 4 which remains using organic solvents, such as a xylene, is removed so that it may be shown, macromolecule resin 3 is removed using PIQ etchant liquid, and manufacture of a semiconductor device is completed.
[0023] At this example, it is drawing 3 (a). Although formed in the front face of the ITO film 9 which formed the low-melting-glass film 6 in the front face of the support substrate 7 in the adhesion process of the support substrate 7 The approach of putting only the ITO layer 9 on the support substrate 7, and forming the low-melting-glass film 6 in the front face of silicon layer 1c is also possible. In this case, drawing 1 (b) It is drawing 1 (a) so that it may be shown. The negative terminal of DC power supply 10 must be conversely connected to the conductive paste 8 formed in the side face of silicon layer 1c.
[0024]
[Effect of the Invention] If the ordinary temperature anode plate conjugation method of this invention is used so that clearly from the above explanation In case the silicon layer which formed and carried out lamination of the semiconductor device is pasted up on a support substrate, air bubbles are not made to mix in a glue line. And become possible to paste up, where

bond strength is raised, and from the low temperature of operating temperature, when the semiconductor device formed in this silicon substrate that carried out lamination is put to the room temperature of non-operating temperature, it is also set. There is an advantage of the silicon substrate which carried out lamination from the support substrate not exfoliating, and offer of the economical [remarkable] and the remarkable manufacture approach of the semiconductor device which can expect the effectiveness of the improvement in dependability is possible.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing showing the example of ordinary temperature anode plate junction of this invention
[Drawing 2] The sectional side elevation showing the manufacture approach of the semiconductor device of one example by this invention in order of a process (1)
[Drawing 3] The sectional side elevation showing the manufacture approach of the semiconductor device of one example by this invention in order of a process (2)
[Drawing 4] Drawing explaining ordinary temperature anode plate junction
[Drawing 5] The sectional side elevation showing the configuration of the conventional semiconductor device
[Description of Notations]
1 SOI Substrate
1a Silicon plate
1b Silicon oxide
1c Silicon layer
2 Semiconductor Device
3 Macromolecule Resin
4 Wax Film
5 Transparence Support Substrate
6 Low-Melting-Glass Film
7 Support Substrate
8 Conductive Paste
9 ITO Film

[Translation done.]

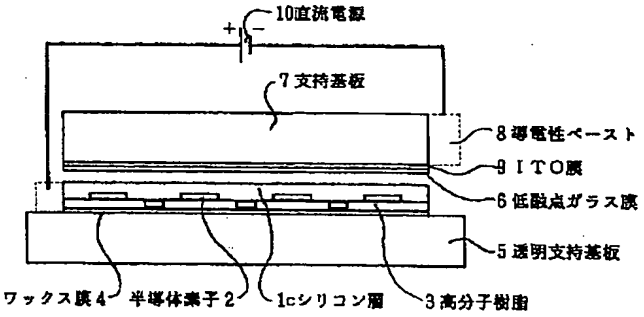
* NOTICES *

DRAWINGS

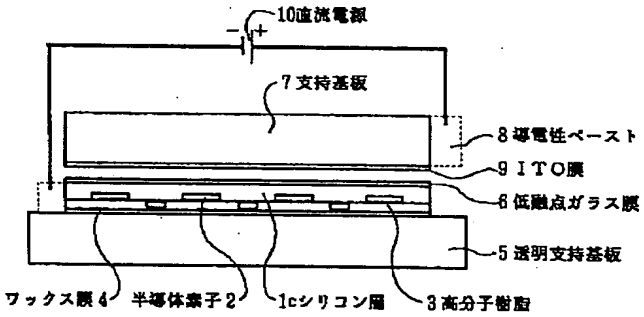
[Drawing 1]

本発明の常温陽極接合の実施例を示す図

(a) 陽極接合状態の一例の構成図



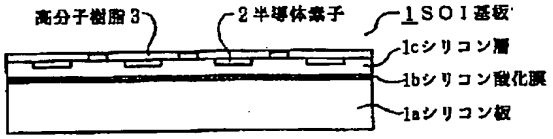
(b) 陽極接合状態の他の例の構成図



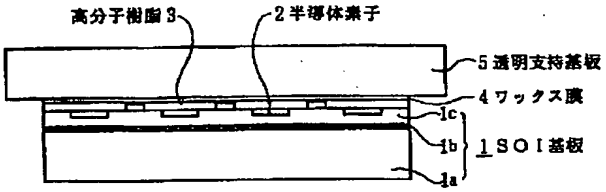
[Drawing 2]

本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(1)

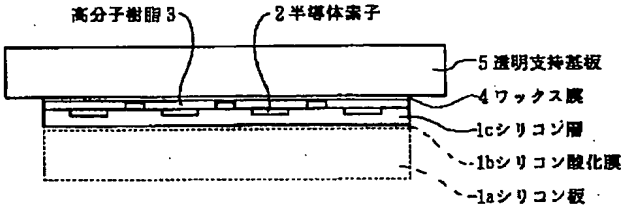
(a) 半導体素子(2) の形および高分子樹脂(3) の塗布



(b) 透明支持基板(5) への貼着

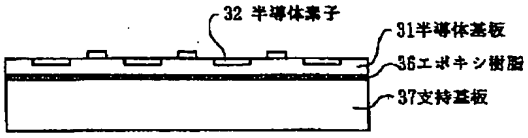


(c) シリコン板(1a)の研磨およびシリコン酸化膜(1b)のエッチング



[Drawing 5]

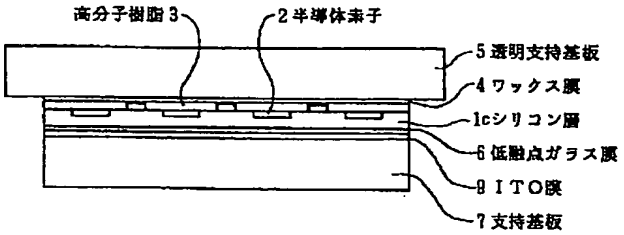
従来の半導体装置の構成を示す側断面図



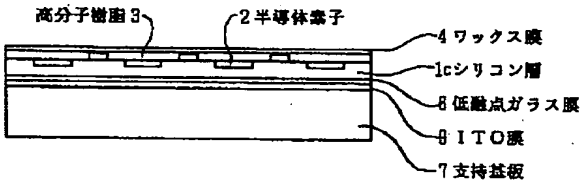
[Drawing 3]

本発明による一実施例の半導体装置の製造方法を工程順に示す断面図(2)

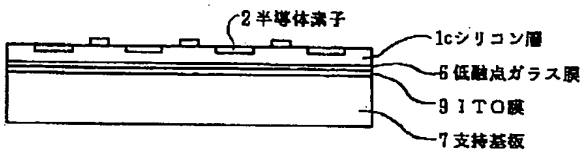
(a) 支持基板(7) の接着



(b) 透明支持基板(5) の剥離

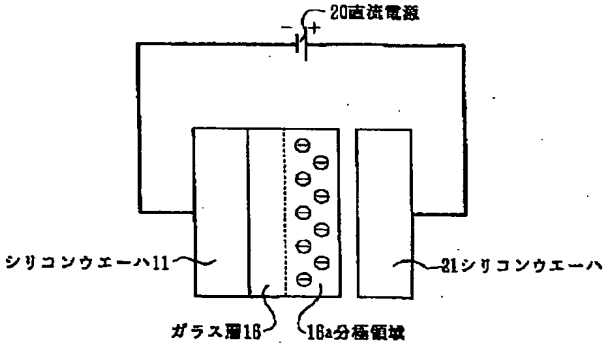


(c) ワックス膜(4) 及び高分子樹脂(3) の除去



[Drawing 4]

常温陽極接合を説明する図



[Translation done.]

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	21/52	Ｃ	7376－4Ｍ			
	27/14					
			7210－4Ｍ	Ｈ０１Ｌ	27/14	Ｋ

審査請求　未請求　請求項の数１　ＯＬ　（全５頁）

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(54)【発明の名称】　半導体装置の製造方法

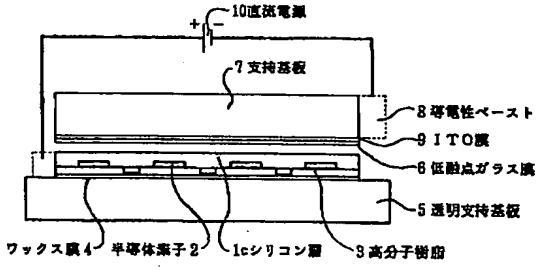
(57)【要約】

【目的】　半導体装置を形成して薄層化した基板を他の支持基板に転写する半導体装置の製造方法に関し、この薄層化した基板を絶縁性の支持基板に気泡などを発生させないで、強固に接着できる半導体装置の製造方法の提供を目的とする。

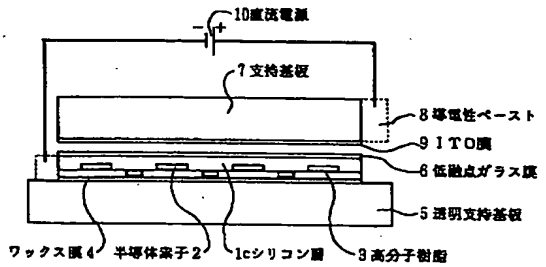
【構成】　ＳＯＩ基板のシリコン層1cの表面に半導体素子２を形成した後、この半導体素子２形成領域に高分子樹脂３を埋設して平坦化し、この高分子樹脂３と透明支持基板５とを接着し、この半導体素子２形成領域と対向する側のこのＳＯＩ基板のこの絶縁体側を研磨してシリコン層1cを薄層化する裏面入射型の赤外線検知素子の製造工程において、薄層化したこのシリコン層1cを、絶縁性を有し且つ赤外線を透過する支持基板７に、低融点ガラス膜６を介して、直流電圧を印加しながら、常温において接合する工程と、この高分子樹脂３からこの透明支持基板５を剥離し、この高分子樹脂３を除去する工程とを含むように構成する。

本発明の常温陽極接合の実施例を示す図

(a) 陽極接合状態の一例の構成図



(b) 陽極接合状態の他の例の構成図



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【特許請求の範囲】

【請求項１】　シリコン基板、或いは絶縁体(1a)上にシリコン層(1c)を設けたＳＯＩ基板(1) の前記シリコン層(1c)の表面に半導体素子(2) を形成した後、該半導体素子(2)形成領域に樹脂(3)を埋設して該半導体素子(2) 形成領域を平坦化し、該半導体素子(2)形成領域を埋設して平坦化した前記樹脂(3)と透明支持基板(5) とを接着し、前記半導体素子(2) 形成領域と対向する側の前記シリコン基板、或いは前記ＳＯＩ基板(1) の前記絶縁体(1a)側を研磨してシリコン層(1c)を薄層化する裏面入射型の赤外線検知素子の製造工程において、

薄層化した前記シリコン基板、或いは前記シリコン層(1c)を、絶縁性を有し且つ赤外線を透過する支持基板(7)に、低融点ガラス膜(6) を介して、直流電圧を印加しながら、常温において接合する工程と、

前記半導体素子(2) を埋設した前記樹脂(3) から前記透明支持基板(5) を剥離し、埋設した前記樹脂(3) を除去する工程と、

を含むことを特徴とする半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は半導体撮像素子や、ポリシリコン等で歯車等の微小機械部品を形成したマイクロマシン等に係り、特に半導体装置を形成して薄層化した基板を他の支持基板に転写する半導体装置の製造方法に関するものである。

【０００２】

【従来の技術】従来はシリコン等の半導体基板にＣＭＯＳ型の半導体素子を形成して赤外線検知素子を製造する場合には、このシリコン基板表面にはシリコン酸化膜や、電極や配線層等が形成されており、このシリコン基板の半導体素子を形成した面側から赤外線を入射すると、上記の配線層や電極で赤外線が遮蔽されて半導体素子形成領域に入射しないので、高感度の赤外線撮像素子を製造するには、シリコン基板の半導体素子を形成していない裏面側より赤外線を入射する裏面入射型の赤外線検知素子が製造されている。

【０００３】しかし、シリコン基板の板厚が厚い場合には、裏面側より入射した赤外線がシリコン基板に吸収され易いので、シリコン基板の板厚は10μｍ 以下に薄くしなければならないが、このようにシリコン基板を10μｍ以下の薄板にすると、割れやすくなり取扱が困難であるという問題が生じている。

【０００４】このため従来は、図５に示すように半導体素子32を形成した板厚が薄い半導体基板31を、赤外線を透過するサファイア等からなる絶縁性の支持基板37にエポキシ樹脂36を用いて接着する方法を採用している。

【０００５】

【発明が解決しようとする課題】以上説明した従来の半導体装置の製造方法においては、上記のように接着剤を

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用いて半導体基板を赤外線を透過するサファイア等からなる絶縁性の支持基板に接着しているが、接着剤を均一に薄く引き伸ばして接着することは技術的に非常に困難であり、また接着剤の内部に気泡が形成され易く、このように半導体基板を支持基板に接着して製造した赤外線撮像素子を、動作温度の液体窒素の温度から動作させていない場合の室内の温度に曝すと、気泡内の空気が温度差によって膨張し、接着剤にひび割れが発生するという問題点があった。

【０００６】本発明は以上のような状況から、半導体素子を形成して薄層化した半導体基板を絶縁性の支持基板に接着する際に、気泡などを発生させないで、強固に接着することが可能となる半導体装置の製造方法の提供を目的としたものである。

【０００７】

【課題を解決するための手段】本発明の半導体装置の製造方法は、シリコン基板、或いは絶縁体上にシリコン層を設けたＳＯＩ基板のこのシリコン層の表面に半導体素子を形成した後、この半導体素子形成領域に樹脂を埋設してこの半導体素子形成領域を平坦化し、この半導体素子形成領域を埋設して平坦化したこの樹脂と透明支持基板とを接着し、この半導体素子形成領域と対向する側のこのシリコン基板、或いはこのＳＯＩ基板の前記絶縁体側を研磨してシリコン層を薄層化する裏面入射型の赤外線検知素子の製造工程において、薄層化した前記シリコン基板、或いは前記シリコン層を、絶縁性を有し且つ赤外線を透過する支持基板に、低融点ガラス膜を介して、直流電圧を印加しながら、常温において接合する工程と、この半導体素子を埋設したこの樹脂からこの透明支持基板を剥離し、埋設したこの樹脂を除去する工程とを含むように構成する。

【０００８】

【作用】即ち本発明においては、半導体層の一方の面に半導体素子を形成した後、薄層化した半導体層と、この半導体層と同様な熱膨張係数を有し、赤外線を透過して絶縁性を有する支持基板とを常温陽極接合により接着するので強固に接着することが可能となり、半導体装置を動作温度の液体窒素温度の77° Ｋから非動作温度の室温に曝す場合においても、この半導体層が支持基板から剥離するのを防止することが可能となる。

【０００９】この常温陽極接合は文献（Sensors and Actuators, A-21-A23(1990)931-934)の"LoW-temperature Silicon-to-silicon Anodic Bonding with Intermediate LowMelting Point Glass, by MASAYOSHI ESASHI, AKIRA NAKANO, SHUICHI SHOJI andHIROYUKI HEBIGUCHI"において開示されている。

【００１０】この文献によれば、この方法は図４に示すように一方のシリコンウエーハ11にガラス層16をスパッタ法で被着し、他方の接着すべきシリコンウエーハ21と対向させて配置し、直流電源20によりガラス層16をスパ

ッタしたシリコンウエーハ11に負の直流電圧が印加されるように電圧を印加すると、印加された直流電圧の電界によってスパッタされているガラス層16の一部に負のイオンが集合して分極領域16a が形成され、正の電圧が印加されている他方のシリコンウエーハ21にこの分極領域内の負のイオンが引きつけられてシリコンウエーハ同士が接着される方法である。

【００１１】本発明においては、この原理を利用し、図１(a) に示すように電圧が確実に印加されるように、支持基板７側が導体になるように支持基板７の表面に導電性で透明なインジウム・錫・酸化物（ＩＴＯ）の膜を被着し、このＩＴＯ膜９の表面に低融点ガラス（PbO-ZnO-B_2O_3）からなる低融点ガラス膜６を被着する。

【００１２】そして支持基板７およびシリコン層1cのそれぞれの側面に導電性ペースト８を塗布し、低融点ガラス膜６を被着した支持基板７側に負の直流電圧が印加されるように電圧を印加して低融点ガラス膜６とシリコン層1cとを圧着すると、支持基板７とシリコン層1cとを接着することが可能である。

【００１３】また図１(b) に示すようにシリコン層1cの表面に低融点ガラス膜６を形成した場合には、直流電圧を図１(a) の場合とは反対にシリコン層1cに負の直流電圧が印加されるように電圧を印加して低融点ガラス膜６とＩＴＯ膜９とを圧着すると、支持基板７とシリコン層1cとを接着することが可能である。

【００１４】この接着に用いる低融点ガラス（PbO-ZnO-B_2O_3）膜の厚さは、樹脂層で接着する場合には実現不可能な１μm 以下の厚さの層で接着することが可能であり、樹脂で接着した場合のように気泡が残留しないので、半導体装置を動作温度の液体窒素温度の77° Kから室温の非動作温度に曝しても剥離することはない。

【００１５】

【実施例】以下図１～図３により本発明のシリコン板上にシリコン層を形成したＳＯＩ基板を用いる一実施例について詳細に説明する。

【００１６】図１は本発明の常温陽極接合の実施例を示す図、図２は本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(1) 、図３は本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(2) である。

【００１７】まず図２(a) に示すように、板厚 400μm のシリコン板1a上に膜厚１μm のシリコン酸化膜1bと膜厚５～15μm のシリコン層1cを形成したＳＯＩ基板１の、シリコン層1c側にＣＭＯＳプロセスで半導体素子２を形成した後、この形成した半導体素子２の形成領域の全面にポリイミド樹脂(日立化成社製、商品名：ＰＩＱ) からなる高分子樹脂３を塗布してこの半導体素子２の形成領域側を平坦にする。

【００１８】つぎに、図２(b) に示すように、この半導体素子２の形成領域を被覆している高分子樹脂３の平坦な表面と、石英からなる透明支持基板５とを加熱し溶融したワックスを用いて接着する。ここで透明支持基板５を用いるのは、ワックス膜４の気泡を見つけて除去し、接着を確実にするためである。

【００１９】ついで図２(c) に示すように、半導体素子２を形成した側の反対側のＳＯＩ基板１のシリコン板1aを約 360μm 研磨してシリコン酸化膜1bに到達する直前で研磨を停止し、ＳＯＩ基板１のシリコン酸化膜1bとの界面に到達するまで苛性カリからなるエッチング液を用いるエッチングか、或いはドライエッチングにより残余のシリコン板1aを除去し、弗化アンモン(NH_4F) と弗酸（ＨＦ）とからなるバッファード弗酸を用いてシリコン酸化膜1bを除去する。

【００２０】ついで図３(a) に示すように、この半導体素子２を形成したシリコン層1cと熱膨張率が合致した、サファイヤからなる支持基板７に導電性を持たせるために、インジウム・錫・酸化物（以下、ＩＴＯと略称する。）からなる膜厚 0.3μm のＩＴＯ層９をスパッタ法により形成し、このＩＴＯ層９の表面に膜厚 0.5μm の低融点ガラス（PbO-ZnO-B_2O_3）膜６をスパッタ法により形成した後、図１(a) に示すようにシリコン層1cの側面と支持基板７の側面に導電性ペースト８を被着させて形成する。

【００２１】前記の低融点ガラス（PbO-ZnO-B_2O_3）膜６を被着した支持基板７に負の直流電圧が印加されるように電圧を印加し、シリコン層1c側に正の直流電圧が印加されるように電圧を印加した状態で直流電源10により数10Ｖの直流電圧を印加すると、支持基板７の表面のＩＴＯ膜９とシリコン層1cとを低融点ガラス膜６を介して強固に接着することが可能となる。この際、基板上に錘を載せて加圧すると、印加電圧を低くすることが可能となる。

【００２２】その後、煮沸した純水中に浸漬してワックス膜４を軟化させ、図３(b) に示すように薄層化したシリコン層1cから透明支持基板５を剥離し、図３(c) に示すようにキシレン等の有機溶剤を用いて残留しているワックス膜４を除去し、ＰＩＱエッチャント液を用いて高分子樹脂３を除去して半導体装置の製造が完了する。

【００２３】本実施例では、図３(a) の支持基板７の接着工程において低融点ガラス膜６を支持基板７の表面に形成したＩＴＯ膜９の表面に形成したが、支持基板７にはＩＴＯ層９のみを被着し、シリコン層1cの表面に低融点ガラス膜６を形成する方法も可能であり、この場合には図１(b) に示すように図１(a) とは逆に、直流電源10の負の端子をシリコン層1cの側面に形成した導電性ペースト８に接続しなければならない。

【００２４】

【発明の効果】以上の説明から明らかなように、本発明の常温陽極接合法を用いると、半導体素子を形成して薄層化したシリコン層を支持基板に接着する際に接着層に

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気泡を混入させず、且つ接着強度を高めた状態で接着することが可能となり、この薄層化したシリコン基板に形成した半導体素子を動作温度の低温から、非動作温度の室温に曝した場合においても、支持基板から薄層化したシリコン基板が剥離しない等の利点があり、著しい経済的及び、信頼性向上の効果が期待できる半導体装置の製造方法の提供が可能である。

【図面の簡単な説明】

【図１】　本発明の常温陽極接合の実施例を示す図

【図２】　本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(1)

【図３】　本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(2)

【図４】　常温陽極接合を説明する図

＊【図５】　従来の半導体装置の構成を示す側断面図

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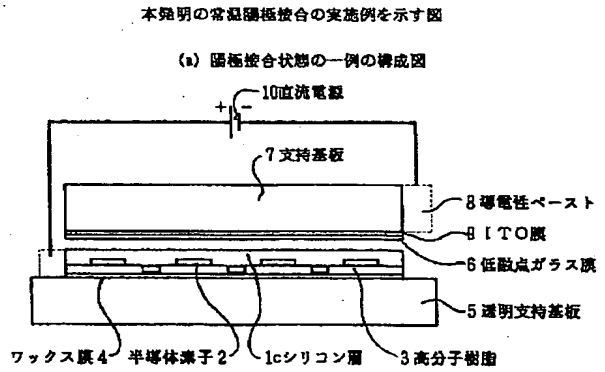
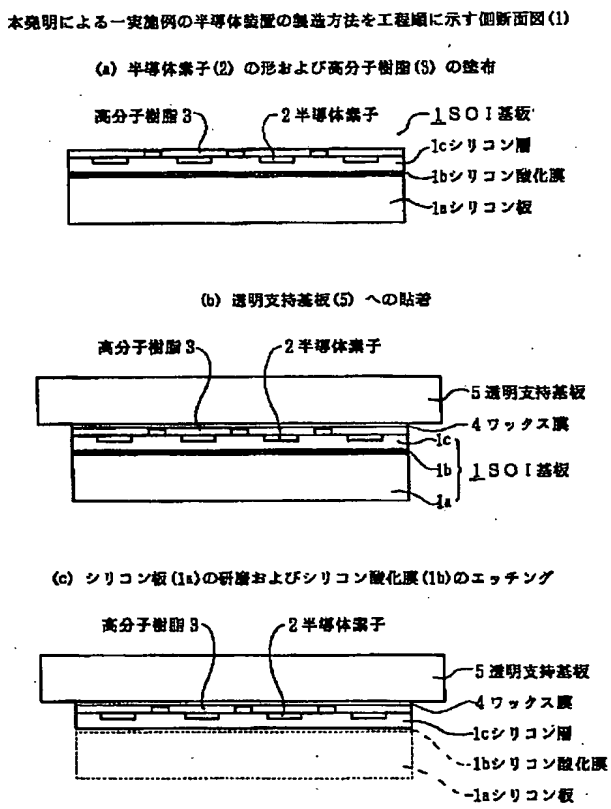
【符号の説明】

1　ＳＯＩ基板
1a　シリコン板
1b　シリコン酸化膜
1c　シリコン層
2　半導体素子
3　高分子樹脂
4　ワックス膜
5　透明支持基板
6　低融点ガラス膜
7　支持基板
8　導電性ペースト
9　ＩＴＯ膜

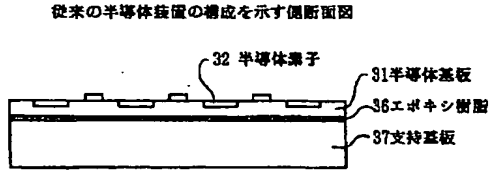
【図１】



【図２】



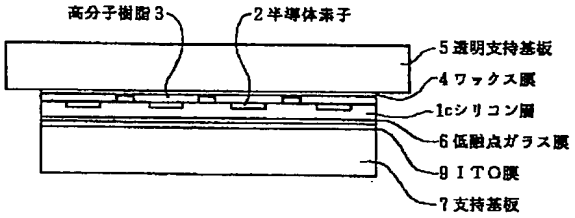
【図５】



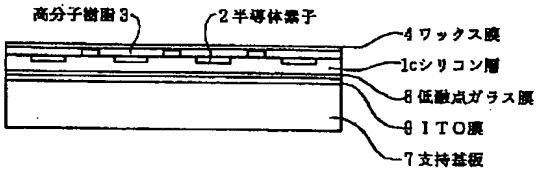
【図３】

本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(2)

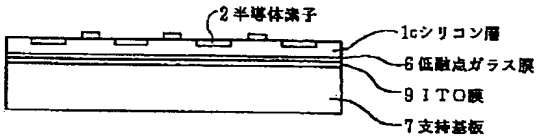
(a) 支持基板(7) の接着



(b) 透明支持基板(5) の剥離



(c) ワックス膜(4) 及び高分子樹脂(3) の除去



【図４】

常温陽極接合を説明する図